

## CLAIMS

What is claimed is:

1. A multithreaded processor supporting a plurality of active threads, the multithreaded processor comprising:
  - an instruction fetch and issue unit comprising
    - an instruction fetch stage configured to fetch a plurality of sets of fetched bits, wherein each set of fetched bits represents one or more instructions; and
    - a pipeline coupled to the instruction fetch and issue unit and configured to receive a set of fetched bits and an associated thread ID.
2. The multithreaded processor of Claim 1, wherein the instruction fetch and issue unit further comprises an instruction buffer coupled to the instruction fetch stage and configured to store the sets of fetched bits and the associated thread ID for each set of fetched bits.
3. The multithreaded processor of Claim 1, wherein the instruction fetch and issue unit further comprises a pre-decode stage configured to pre decode each set of fetched bits.
4. The multithreaded processor of Claim 1, wherein the pipeline further comprises a plurality of pipeline stages, wherein each pipeline stage stores a thread ID.
5. The multithreaded processor of Claim 3, wherein the pipeline further comprises a data forwarding unit for forwarding data from a first pipeline stage having a first thread ID to an second pipeline stage having a second thread ID.

6. The multithreaded processor of Claim 5, wherein the data forwarding unit comprises a thread ID comparator.

7. The multithreaded processor of Claim 5, wherein the data forwarding unit forwards data when the first thread ID is equal to the second thread ID.

8. The multithreaded processor of Claim 5, wherein the data forwarding unit prevents data forwarding when the first thread ID is not equal to the second thread ID.

9. The multithreaded processor of Claim 1, further comprising a trap handler.

10. The multithreaded processor of Claim 9, wherein the trap handler resolves a first trap having a first thread ID when the active thread corresponds to the first thread ID.

11. The multithreaded processor of Claim 9, wherein the trap handler suspends a first trap having a first thread ID when the active thread does not correspond to the first thread ID.

12. A method of operating a multithreaded processor supporting a plurality of threads, the method comprising:

    fetching a first set of fetched bits representing one or more instructions;

    attaching an associated thread ID to the set of fetched bits; and

    issuing the instructions of the first set of fetched bits with the associated thread ID to a pipeline.

13. The method of Claim 12, further comprising:

reading a first operand for the first set of instructions;  
and

propagating the associated thread ID through the  
pipeline with the first set of instructions and operand.

14. The method of Claim 12, further comprising storing the associated thread ID in a thread ID memory in each stage of the pipeline operating on an instruction from the first set of instructions.

15. The method of Claim 12, further comprising forwarding data from a first pipeline stage to a second pipeline stage when a first thread ID in the first pipeline stage is equal to a second thread ID in the second pipeline stage.

16. The method of Claim 12, further comprising preventing data forwarding from a first pipeline stage to a second pipeline stage when a first thread ID in the first pipeline stage is not equal to a second thread ID in the second pipeline stage.

17. The method of Claim 12, further comprising storing an active thread ID of an active thread as a trap thread ID when a trap is detected.

18. The method of Claim 17, further comprising preventing trap resolution when the trap thread ID does not equal the active thread ID.

19. The method of Claim 17, further comprising resolving a trap when the trap thread ID equals the active thread ID.

20. A multithreaded processor supporting a plurality of threads comprising:

means for fetching a first set of fetched bits representing one or more instructions;

means for attaching an associated thread ID to the set of fetched bits; and

means for issuing the instructions of the first set of fetched bits with the associated thread ID to a pipeline.

21. The multithreaded processor of Claim 20, further comprising:

means for reading a first operand for the first set of instructions; and

means for propagating the associated thread ID through the pipeline with the first set of instructions and operand.

22. The multithreaded processor of Claim 20, further comprising means for storing the associated thread ID in a thread ID memory in each stage of the pipeline operating on an instruction from the first set of instructions.

23. The multithreaded processor of Claim 20, further comprising means for forwarding data from a first pipeline stage to a second pipeline stage when a first thread ID in the first pipeline stage is equal to a second thread ID in the second pipeline stage.

24. The multithreaded processor of Claim 20, further comprising means for preventing data forwarding from a first pipeline stage to a second pipeline stage when a first thread ID in the first pipeline stage is not equal to a second thread ID in the second pipeline stage.

25. The multithreaded processor of Claim 20, further comprising means for storing an active thread ID of an active thread as a trap thread ID when a trap is detected.

26. The multithreaded processor of Claim 25, further comprising means for preventing trap resolution when the trap thread ID does not equal the active thread ID.

27. The multithreaded processor of Claim 25, further comprising means for resolving a trap when the trap thread ID equals the active thread ID.